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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,358	05/17/2007	Kenichi Kagawa	10294.0003	6738

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EXAMINER	
SKYLES, TIFNEY L	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,358	KAGAWA ET AL.	
	Examiner	Art Unit	
	TIFNEY L. SKYLES	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *13 and 15-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-18* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6-10, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Combi et al (US 2004/0157364 A1).

Regarding Claim 1, Combi et al teach a semiconductor device cut into respective chips by a dicing process, comprising: a substrate **2a** [Fig. 27] having an edge along a dicing line; a semiconductor element **SB** (shown in Fig. 20) formed on said substrate **2a**; a jetty portion **C** (shown in Fig. 20) formed between said semiconductor element **SB** and said edge on said substrate **2a** and having a laminated structure and including an insulating layer **13a** and a conducting layer **15b** formed on said insulating layer **13a**; and an electrode pad **16'** for signal input and output which is formed on said semiconductor element **SB**, and inside of the outermost wall of said jetty portion **C**.

Regarding Claim 2, Combi et al teach the semiconductor device according to claim 1, wherein said jetty portion **C** continuously extends along said edge in parallel.

Regarding Claim 3, Combi et al teach the semiconductor device according to claim 1, wherein said jetty portion **C** is formed so as to surround periphery of said semiconductor element **SB**.

Regarding Claim 4, Combi et al teach semiconductor device according to claim 1, wherein said semiconductor element **SB** includes an insulating layer **13a** and a conducting layer **15b** formed on said insulating layer **13a**; said insulating layer **13a** of said semiconductor element **SB** and said insulating layer **13a** of said jetty portion **C** are formed in the same process; and said conducting layer **15b** of said semiconductor element **SB** and said conducting layer **15b** of said jetty portion **C** are formed in the same process.

Regarding Claim 6, Combi et al teach a semiconductor device comprising: a substrate **2a**; a structure body **SB** supported by a fixing portion so as to form a space between said substrate **2a** and said structure body **SB**; and a jetty portion **C** formed on said substrate **2a** between the outer periphery of said substrate **2a** and a portion of said structure body **SB** which is not supported by said fixing

portion, including an insulating layer **13a** and a conducting layer **15b** formed on said insulating layer **13a**.

Regarding Claim 7, Combi et al teach the semiconductor device according to claim 6, wherein a plurality of said jetty portions **C** are formed so as to surround the outer periphery of said structure body **SB**.

Regarding Claim 8, Combi et al teach semiconductor device according to claim 6 further comprising an electrode pad **16'** for signal input and output which is formed on said structure body **SB** and inside of the outermost wall of said jetty portion **C**.

Regarding Claim 9, Combi et al teach the semiconductor device according to claim 8, wherein a plurality of said jetty portions **C** are formed so as to surround said structure body **SB** and said electrode pad **16'** for signal input and output is arranged inside of an imaginary outer periphery which is formed by connecting the outermost walls of said jetty portions **C**.

Regarding Claim 10, Combi et al teach the semiconductor device according to claim 6, wherein said structure body **SB** includes a conducting layer **10** [Fig. 10] formed on said fixing portion; said fixing portion of said structure body **SB** and said insulating layer of said jetty portion **C** are formed in the same process; and

said conducting layer **15b** of said structure body **SB** and said conducting layer **15b** of said jetty portion **C** are formed in the same process.

Regarding Claim 14, Combi et al teach the semiconductor device according to claim 6, wherein an upper portion of inside area of said jetty portion **C** is opened.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Combi et al in view of Mlcak et al (US 2003/0119220 A1).

Regarding Claim 5, Combi et al teach the semiconductor device according to claim 1, wherein said electrode pad **16'** for signal input and output is formed on said conducting layer **12a** of said semiconductor element **SB**, and wherein said jetty portion **C** includes a conducting layer **15b** [Fig. 10] but fail to teach an electrode pad for said jetty portion which is formed inside of said outermost wall on said conducting layer of the jetty portion, and which is connected electrically to said electrode pad for signal input and output in order to make potential difference between said conducting layer of said jetty portion and said conducting layer of said semiconductor element close to zero. However, Mlcak et al teach an electrode pad **24** [Fig. 1B] which is formed inside of said outermost wall on said conducting layer **14**, and which is connected electrically **44** to said electrode pad for signal input and output in order to make potential difference between said conducting layer **14** and said conducting layer **12** of said semiconductor element **11** close to zero. Therefore, it would have been obvious to a person having ordinary skill in the art to combine Combi et al with Mlcak et al because it will improve functionality that is capable of operating at higher temperatures and in more corrosive environments [Para. 0004].

Regarding Claim 11, Combi et al teach the semiconductor device according to claim 10, wherein said electrode pad **16'** for signal input and output is formed on said conducting layer **12a** of said structure body **SB** but fail to teach said

semiconductor device further comprising an electrode pad for said jetty portion which is formed on said conducting layer of said jetty portion, and which is connected electrically to said electrode pad for signal input and output in order to make potential difference between said conducting layer of said jetty portion and said conducting layer of said structure body close to zero. However, Mlcak et al teach said semiconductor device further comprising an electrode pad **24** [Fig. 1B] formed on said conducting layer **14**, and which is connected electrically **44** to said electrode pad for signal input and output in order to make potential difference between said conducting layer **14** and said conducting layer **12** of said structure body **11** close to zero. Therefore, it would have been obvious to a person having ordinary skill in the art to combine Combi et al with Mlcak et al because it will improve functionality that is capable of operating at higher temperatures and in more corrosive environments [Para. 0004].

Regarding Claim 12, Combi et al teach the limitations of claim 10 but fail to teach the semiconductor device according to claim 10 further comprising a potential equalizer in order to make potential difference between said conducting layer of said jetty portion and said conducting layer of said structure body close to zero. However, Mlcak et al teach the semiconductor device according to claim 10 further comprising a potential equalizer **44** [Fig. 1B] in order to make potential difference between said conducting layer and said conducting layer of said structure body close to zero. Therefore, it would have been obvious to a person

having ordinary skill in the art to combine Combi et al with Mlcak et al because it will improve functionality that is capable of operating at higher temperatures and in more corrosive environments [Para. 0004].

Response to Arguments

6. Applicant's arguments filed 10/29/2008 have been fully considered but they are not persuasive. The Applicant argues that Combi fails to teach claimed "jetty portion" however if one looks closely at Figure 27 one will see that "a jetty portion...including an insulating layer and a conducting layer formed on said insulating layer" is illustrated. Therefore the rejection still stands. The Applicant also argues that Combi is not prior art under 102(b) because the national stage application was filed February 28, 2005 wherein Combi's publication date is August 12, 2004. The Applicant is correct on this matter and the appropriate corrections have been made.

7. The Examiner acknowledges the Applicant's amendment of the title.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIFNEY L. SKYLES whose telephone number is (571)270-5019. The examiner can normally be reached on Mon-Fri 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

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